Pooneh Safayenikoo <psafayen@ucsc.edu>

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RESEARCH INTERESTS

- Disaggregated Computing, Computer Architecture, Machine Learning, Operating Systems

EDUCATION

University of California Santa Cruz   *September 2021-Present*
Ph.D. in Computer Science and Engineering

- Research Title: "Memory Allocation for Disaggregated Computing" under supervision of Dr. Andrew Quinn

University of Missouri   *Transferred to University of California Santa Cruz*
Ph.D. in Computer Science and Engineering

- M.Sc Thesis Title: "Neural Network Accelerator Optimization" under supervision of Dr. Ismail Akturk

Iran University of Science and Technology
M.Sc. in Computer Engineering

- Thesis Title: "Data Coding in Energy-efficient Hybrid Uncore Structure for 3D Chip-Multiprocessors" under supervision of Dr. Mahmood Fathy

Ferdowsi University of Mashhad
B.Sc. in Computer Engineering

- Thesis Title: "Head Tracking and Pose Estimation" under supervision of Dr. Hamid Reza Pourreza

PATENT

- Woo SC, Vogelsang T, Tringali JJ, **Safayenikoo P**, inventors; Rambus Inc, assignee. Dynamic processing speed. United States patent application US 17/504,739. 2022 May 5.

PUBLICATION

- Yang, Yiwei, **Pooneh Safayenikoo**, Jiacheng Ma, Tanvir Ahmed Khan, and Andrew Quinn. "CXLMemSim: A pure software simulated CXL. mem for performance characterization." arXiv preprint arXiv: 2303.06153 (2023).
- **Pooneh Safayenikoo**, and Ismail Akturk, "Weight Update Skipping: Reducing Training Time for Artificial Neural Networks," in IEEE Journal on Emerging and Selected Topics in Circuits and Systems, vol. 11, no. 4, pp. 563-574, Dec. 2021, doi: 10.1109/JETCAS.2021.3127907.
- **Pooneh Safayenikoo**, Arghavan Asad, Mahmood Fathy, "Energy-efficient Non Uniform Last Level Caches for Chip-multiprocessors Based on Compression.", arXiv preprint.
- **Pooneh Safayenikoo**, Arghavan Asad, Mahmood Fathy, Farah Mohammad, "NIZCache: Energy-efficient Non-uniform Cache Architecture for Chip-multiprocessors Based on Invalid and Zero Lines." In Circuits and Systems (ISCAS), 2018, pp. 1-5.
- **Pooneh Safayenikoo**, Arghavan Asad, Farah Mohammad,"Energy-efficient Cache Architecture for Chip-multiprocessors Based on Non-uniformity Accesses", CCECE, 2018.
- **Pooneh Safayenikoo**, Arghavan Asad, Mahmood Fathy, Farah Mohammad, "An energy efficient non-uniform Last Level Cache Architecture in 3D chip-multiprocessors," in Quality Electronic Design (ISQED), 18th International Symposium on, 2017, pp. 373-378.
- **Pooneh Safayenikoo**, Arghavan Asad, Mahmood Fathy, Farah Mohammad, "Exploiting the Non-uniformity of Write Accesses to Design High-Endurance Hybrid Last Level Cache in 3D CMP", CCECE, 2017.
- **Pooneh Safayenikoo**, Arghavan Asad, Mahmood Fathy, Farah Mohammad, "A New Traffic Compression Method for End-to-End Memory Access in 3D Chip-multiprocessors", CCECE, 2017.
- **Pooneh Safayenikoo**, Arghavan Asad, Kaamran Raahemifar, Mahmood Fathy, "UCA: An Energy-efficient Hybrid Uncore Architecture in 3D Chip-Multiprocessors to minimize crosstalk," in Proceedings of the 9th International Workshop on Network on Chip Architectures (NoCArc@MICRO), 2016, pp. 39-44.

PRESENTATIONS
- Poster Presentation on THINKLab From Emerging to Pervasive AI, IBM, October 2019.
- Poster Presentation on The First Young Architect Workshop (YArch), HPCA, February 2019.

EXPERIENCE

Engineering Intern   *Summer 2020*
Rambus
- Create and analyze new memory system architectures and devices that improve the performance and power efficiency of machine learning applications resulted in a patent application

Research Assistant
- Center for Research in Storage Systems (CRSS), University of California Santa Cruz
    - Charactizing realistic benchmarks for realistic disaggregated computing
    - Developing application-level mechanisms to enable prefetching or allocation for CXL/far memory
- Emerging Computer Architecture and System Technologies Lab, University of Missouri
    - Performed research on compression methods for last level cache of CMPs
    - Developed energy-aware training for neural networks
- HPC Lab, Iran University of Science and Technology
    - Developed a compression mechanism for networks on chip and last level cache
    - Developed a new mechanism called Selective Compression Architecture (SCA) to reduce delay overhead and static energy from compression/decompression
    - Exploring the role of the compression in the dark silicon and the advantage of storing compressed data to power-off the SRAM cache banks

Teaching Assistant
- Principles of Computer Systems Design, Winter 2023, University of California Santa Cruz
- Computer Architecture, Fall 2020/Spring 2021, University of Missouri
- Computer Architecture, Spring 2018, Ferdowsi University of Mashhad

Peer Review
- ETRI Journal
- IEEE Access Journal

SKILLS
- Programming: C, C++, awk, Matlab, Python, Verilog and VHDL, OpenCV, PyTorch, Tensorflow
- Simulators: (SimpleScalar, Gem5) for performance, and NS2.
- Tools: Linux Perf, VTune, Synopsys-Design Compiler, and HSpice.

COURSE PROJECT
- Application of Supervised Learning for Efficient Classification of Breast Cancer Patients (Supervised Learning)
- Evaluation of Unsupervised Clustering Algorithms (Neural Networks)
- Implementation of Convolutional Neural Network and Deconvolution using linear algebra library for MNIST dataset (Neural Networks)
- The Fittest Mario: An Evolutionary Computation Approach to Super Mario Brothers (Introduction to Computational Intelligence)
- Fault Injection: sim-outorder in SimpleScalar/PISA (Reliable System Design)
- Simulating Mobile Ad hoc Networks using NS2 (Advanced Computer Networks)
- Analyze the power of a case-study interconnect using HSPICE (Low Power Digital System Design)

AWARDS AND HONORS
- Computer Science and Engineering Regents Fellowships (UCSC), 2021
- ISCA 2019 Student Travel Grant Award
- NSF Student Travel Grant Award for HPCA/CGO/PPoPP'19
- Top Student Award in Computer Architecture from Iran University of Science and Technology
- Ranked 89 Nationwide Entrance Exam for M.Sc. studies in Computer Engineering among 30,000 students (Iran)

- Top 1.5% Nationwide Entrance Exam of Iranian Universities, very competitive with nearly 308,875 participants

REFERENCES

- Dr. Andrew R. Quinn, Assistant Professor at the University of California, Santa Cruz, aquinn1@ucsc.edu.
- Dr. Steven Woo, Fellow and Distinguished Inventor at Rambus, swoo@rambus.com
- Dr. Ismail Akturk, Assistant Professor at Electrical Engineering and Computer Science Department (EECS), akturki@missouri.edu.